REMARKS

This is responsive to the Action in this case of June 3, 2002. All pending Claims 1-18 stand rejected; reconsideration is requested.

Claims 1-14 stand rejected under 35 U.S.C. §112. The language cited by the Examiner has been deleted from each of Claims 1 and 9, which as amended instead recite (1) "a second deposited insulative layer" (emphasis added) and (2) "whereby formation of said second insulative layer does not introduce substantial stress in said substrate." Hence the rejection is overcome. The "whereby" clause is descriptive of the "second deposited insulative layer" and is not per se a structural limitation.

Claims 1-18 stand rejected under 35 U.S.C. §102(e) as anticipated by Hshieh. Independent Claims 1, 9, 15, and 17 are each amended to recite "a second deposited insulative layer." (The other amendments to Claims 1-4 and 7-18 other than those discussed above are not in response to a patentability rejection, and are to improve the form of the claims and not to narrow them.)

A relevant part of Hshieh is at column 5 lines 44-54:

> In FIG. 3C, a sacrification oxidation process is applied which can be either a dry or wet oxidation process conducted at a temperature of 900-1100°C to form oxide layer of approximately 300-2000 Å in thickness which is followed by a scarification oxide etch process. A gate oxidation process is then carried out to form an insulation layer 120`, which is preferably a thick-gate-oxide layer 120`. The gate oxidation process can be either a wet or a dry oxidation process carried out at a temperature of 800 to 1100° C to form a thick-gate-oxide layer of thickness in the range between 400 Å to 4,000Å.

LAW OFFICES OF
SKJERVEN MORRILL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

Hence, Hshieh's "thick-gate-oxide-layer 120`" (see Hshieh Figs. 2A and 3C) is conventionally grown thermally i.e. (at high temperature). Of course, this approach is contrary to that disclosed in the present application, see page 6, lines 26-33:

> The N+ implantation is carried out with an arsenic or phosphorus ion beam 114 at energy of 40-100 Kev and ion flux density of $5x10^{15}$ to $1x10^{16}/cm^2$. Referring to FIG 3K, the resist, i.e., the N+ blocking mask 135, is stripped and the N+ source regions 140 are driven into desired junction depth ranging from 0.2 to 1.0 m by a diffusion process at a temperature of 900-1000°C. for 10 minutes to two hours.

It is respectfully pointed out that in this context "deposited" is more than a product-by-process feature, but refers to a structurally different type of oxide layer due to the substantial reduction of stress in the resulting device, which is an observable feature. The specification at page 6, line 32 to page 7, line 6, describes the undesirable structural artifacts - bird's beak, shifts in the etched trench sidewall, and the "bulb" effect - caused by the stress of the conventional growing the thick oxide layer. These stress-related features are avoided or reduced by depositing the gate insulative layer, in accordance with the present invention.

Hence, Claims 1, 9, 15, and 17, each of which now recites "a second deposited insulative layer" are not met by Hshieh, nor suggested by Hshieh, and hence distinguish thereover.

New dependent Claims 30 and 31 are directed to the embodiment where the first insulative layer (e.g., gate oxide) is thermally grown and the second such layer (e.g., thick gate oxide) is deposited. Again, Hshieh fails to disclose or suggest using two different processes to form his gate oxide, and hence Claims 30 and 31 additionally distinguish over Hshieh.

LAW OFFICES OF
SKJERVEN MORRILL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

The remaining claims are also dependent on Claims 1, 9, 15, and 17 and hence allowable for at least the same reason as the base claim, so it is requested that this case pass to issue with all pending Claims 1-18 and 30-31 allowed.

EXPRESS MAIL LABEL NO:

EV 180 324 337 US

Respectfully submitted,

Norman R. Klivans

Norman R. Klivans
Attorney for Applicant(s)
Reg. No. 33,003

LAW OFFICES OF
SKJERVEN MORRILL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

Version with markings to show changes made

1. (amended) A metal-insulator-semiconductor device, comprising:

a semiconductor substrate [including] defining a trench extending into said substrate from a surface of said substrate;

a source region of a first conductivity type adjacent to a sidewall of said trench and to said surface;

a body region of a second conductivity type opposite to said first conductivity type adjacent to said source region and to said sidewall; and

a drain region of said first conductivity type adjacent to said body region and to said sidewall,

[wherein a stress in said substrate along a bottom portion of said trench does not change appreciably and] wherein said trench is lined with a first insulative layer along a portion of said sidewall that abuts said body region and wherein said trench is lined with a second deposited insulative layer along said bottom portion of said trench, said second insulative layer being [coupled to] in contact with said first insulative layer and said second insulative layer being thicker than said first insulative layer, whereby formation of said second insulative layer does not introduce substantial stress in said substrate.

2. (amended) The MIS device of Claim 1, further comprising a gate adjacent [region coupled] to said first insulative layer and said second insulative layer within said trench.

3. (amended) The MIS device of Claim 2, wherein said gate [region] comprises polysilicon.

LAW OFFICES OF
SKJERVEN MORRILL LLP
25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

4. (amended) The MIS device of Claim 1, further including a high conductivity region of said first conductivity type [formed] in said drain region adjacent to at least said bottom portion of said trench.

5. The MIS device of Claim 1, wherein said first insulative layer comprises an oxide.

6. The MIS device of Claim 1, wherein said second insulative layer comprises an oxide.

7. (amended) The MIS device of Claim 1, wherein said second insulative layer [comprises] is a multi-layer insulative layer.

8. (amended) The MIS device of Claim 1, wherein said MIS device [comprises] is a MOSFET.

9. (amended) A trench-gate device [MOSFET], comprising:

a semiconductor substrate [including] defining a trench extending into said substrate from a surface of said substrate;

a source region of a first conductivity type adjacent to a sidewall of said trench and to said surface;

a body region of a second conductivity type opposite to said first conductivity type adjacent to said source region and to said sidewall;

a drain region of said first conductivity type adjacent to said body region and to said sidewall,

[wherein a stress in said substrate along a bottom portion of said trench does not change appreciably and] wherein said trench is lined with a first insulative layer along a portion of said sidewall that abuts said body region and wherein said trench is lined with a second deposited insulative layer along said bottom portion of said trench,

LAW OFFICES OF
SKJERVEN MORRILL LLP
25 METRO DRIVE
SUITE 700
SAN JOSE, CA. 95110
(408) 453-9200
FAX (408) 453-7979

said second insulative layer being [coupled to] in contact with said first insulative layer and said second insulative layer being thicker than said first insulative layer; whereby formation of said second insulative layer does not introduce substantial stress in said substrate; and

a gate [region coupled] adjacent to said first insulative layer and said second insulative layer within said trench.

10. (amended) The trench-gate [MOSFET] device of Claim 9, wherein said gate [region] comprises polysilicon.

11. (amended) The trench-gate [MOSFET] device of Claim 9, further including a high conductivity region of said first conductivity type [formed] in said drain region adjacent to at least said bottom portion of said trench.

12. (amended) The trench-gate [MOSFET] device of Claim 9, wherein said first insulative layer comprises an oxide.

13. (amended) The trench-gate [MOSFET] device of Claim 9, wherein said second insulative layer comprises an oxide.

14. (amended) The trench-gate [MOSFET] device of Claim 9, wherein said second insulative layer [comprises] is a multi-layer insulative layer.

15. (amended) A trench-gate [MOSFET] device, comprising:

a semiconductor substrate [including] defining a trench extending into said substrate from a surface of said substrate;

a source region of a first conductivity type adjacent to a sidewall of said trench and to said surface;

a body region of a second conductivity type opposite to said first conductivity type adjacent to said source region and to said sidewall;

LAW OFFICES OF
SKJERVEN MORRILL LLP
25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

a drain region of said first conductivity type adjacent to said body region and to said sidewall;

a first insulative layer lining said trench along a portion of said sidewall that abuts said body region;

a second deposited insulative layer lining said trench along a bottom portion of said trench, said second insulative layer being thicker than said first insulative layer and said second insulative layer being [coupled to] in contact with said first insulative layer, whereby formation of said second insulative layer does not introduce substantial stress in said substrate;

wherein a thickness of a transition insulative layer at the juncture of said first insulative layer and said second insulative layer is not less than a thickness of said first insulative layer; and

a gate [region coupled] adjacent to said first insulative layer and said second insulative layer within said trench.

16. (amended) The trench-gate [MOSFET] device of Claim 15, further including a high conductivity region of said first conductivity type [formed] in said drain region adjacent to at least said bottom portion of said trench.

17. (amended) A trench-gate [MOSFET] device, comprising:

a semiconductor substrate [including] defining a trench extending into said substrate from a surface of said substrate;

a source region of a first conductivity type adjacent to a sidewall of said trench and to said surface;

a body region of a second conductivity type opposite to said first conductivity type adjacent to said source region and to said sidewall;

LAW OFFICES OF
SKJERVEN MORRILL LLP
25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

a drain region of said first conductivity type adjacent to said body region and to said sidewall;

a first insulative layer lining said trench along a portion of said sidewall that abuts said body region;

a second deposited insulative layer lining said trench along a bottom portion of said trench, said second insulative layer being thicker than said first insulative layer and said second insulative layer being [coupled to] in contact with said first insulative layer, whereby formation of said second insulative layer does not introduce substantial stress in said substrate;

wherein a [first diameter] width of said trench [taken] at a vertical midpoint of said second insulative layer is not greater than a [second diameter] width of said trench [taken] adjacent to said body region; and

a gate [region coupled] adjacent to said first insulative layer and said second insulative layer within said trench.

18. (amended) The trench-gate [MOSFET] device of Claim 17, further including a high conductivity region of said first conductivity type [formed] in said drain region adjacent to at least said bottom portion of said trench.

Please add Claims 30-31:

--30. The MIS device of Claim1, wherein the first insulative layer is thermally grown.

31. The MIS device of Claim 9, where in the first insulative layer is thermally grown. --

LAW OFFICES OF
SKJERVEN MORRILL LLP
25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979